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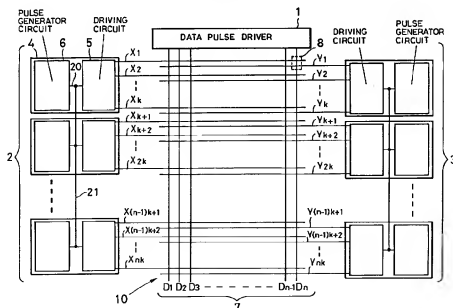
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(54) Driving apparatus for plasma display panel

(57) Disclosed is a driving apparatus for a plasma display panel comprising a group of pairs of row electrodes divided into a plurality of sub-blocks, and a driving pulse generator provided in each sub-block for supplying a driving pulse to the associated sub-block, thereby eliminating non-uniform luminance distribution on the display surface due to variations in voltage of

pulses supplied to row electrode in the respective sub-blocks. Output terminals of the pulse generators in the respective sub-blocks are connected to each other to make the voltage levels of at least sustain pulses constant.

FIG.1



Description

SUMMARY OF THE INVENTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates to a driving apparatus for a plasma display panel.

2. Description of the Related Art

[0002] A plasma display panel (designated as "PDP" hereinafter) is known as an image display that provides a reduction in its thickness and an increase in its screen size. The PDP has a number of effective features not found in conventional CRT displays. There is a need for a reduction in manufacturing cost and an improved quality of the plasma display panel.

[0003] Generally, a PDP comprises a plurality of row electrodes arranged in parallel and a plurality of column electrodes extending perpendicularly to the row electrodes. A display cell is provided at each point of the row and column electrodes. Particularly, in a color type of PDP, an additional row electrode is arranged near the row electrode to be paired so as to prevent fluorescent layer in the cell from wearing due to ion impact. Surface discharge between the pair of row electrodes is utilized as a light source for the color type of PDP.

[0004] The PDP described above requires a plurality of electrodes and a driving circuit for controlling the display for every cell. For providing a PDP having a larger screen size, an immense amount of discharge current is required. Particularly, the integration of the plurality of driving circuits into one chip requires an IC having a large capacity of power supply. Thus, this is not practical in terms of heat generation and manufacturing cost. To overcome the above problem, a conventional PDP driving apparatus divides the group of pairs of row electrodes into a plurality of sub-blocks in order to reduce a load on one IC. Each of sub-blocks then includes one pulse generator. In addition, a driving apparatus is provided for selectively relaying output pulses from the pulse generator.

[0005] However, if there is some difference between impedance and output level of pulses of the pulse generators, the levels of pulses supplied from the driving circuits to the pair of row electrodes may differ from one sub-block to another. In such a case, a problem arises in that a luminance distribution is not uniform on the display surface of the PDP.

OBJECT OF THE INVENTION

[0006] A main object of the present invention is to provide a driving apparatus for a plasma display panel wherein a pulse generator in every sub-block supplies a uniform output level to the corresponding row electrodes.

[0007] The foregoing and other problems are overcome and the object of the invention is realized by an apparatus in accordance with embodiments of the invention. The present invention features a driving apparatus for a plasma display panel comprising: a group of row electrodes including a plurality of pairs of row electrodes, said group of row electrodes being divided into a plurality of sub-blocks, each of which includes a plurality of row electrode pairs; a group of column electrodes including a plurality of column electrodes extending perpendicularly to said group of row electrodes; a pulse generator provided in each of said sub-blocks for generating a sustain pulse; and an electrode driving circuit provided in each of said sub-blocks for selectively relaying said sustain pulse supplied from an output terminal of said pulse generator to apply the relayed sustain pulse to row electrodes in said each sub-blocks, wherein each of said pulse generators has the output terminal connected to the rest of said pulse generators. Thus, the output levels of pulses supplied from the pulse generators equals to each other.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The aforementioned aspects and other features of the invention are explained in the following description, taken in connection with the accompanying drawing figures wherein:

Fig. 1 is a schematic view illustrating a structure of a driving apparatus including a plurality of sub-blocks for a plasma display panel according to the present invention;

Fig. 2 is circuit diagram illustrating one embodiment of the driving apparatus of Fig. 1; and

Figs. 3A and 3B illustrate waveforms of sustain pulses supplied from the pulse generator of Fig. 2.

DESCRIPTION OF PREFERRED EMBODIMENTS

[0009] A preferred embodiment of the present invention will be described with reference to the accompanying drawings. Referring to Fig. 1, a PDP comprises a group of X-row electrodes 2 including a plurality of row electrodes X_1, X_2, X_3, \dots ; a group of Y-row electrodes 3 including a plurality of row electrodes Y_1, Y_2, Y_3, \dots , each of which forms a pair with a corresponding one of the X-row electrode group; and a group of column electrodes 7 including a plurality of column electrodes D_1, D_2, D_3, \dots , which are orthogonal to the X-row electrode group 2 and the Y-row electrode group 3. A display cell 8 is formed at each intersection of the pair of row electrodes and the column electrode. The X-row electrode group 2 is divided into η sub-blocks, each of which includes k row electrodes. The Y-row electrode group 3 is divided into η sub-blocks, each of which includes k

row electrodes. A pulse generator 6 is provided in each sub-block for generating a priming (discharge starting) pulse and a sustain pulse. The pulse generator 6 and a driving circuit 5 constitutes an electrode driving circuit 4. The driving circuit 5 selects one of the priming pulse and the sustain pulse from the pulse generator 6 to translate the selected one to the row electrodes. The driving circuit 5 also generates a scanning pulse to supply the scanning pulse to the associated row electrode. The driving circuit 5 is connected to the pulse generator 6 through a lead 20. Fig. 2 illustrates one example of a circuit diagram of the driving circuit 5 and the pulse generator 6. Further, the lead line 20 of each sub-block is interconnected through an equipotential line 21.

[0010] Fig. 2 illustrates the circuit diagram of the driving circuit 5 and the pulse generator 6 for generating the scanning pulse, the priming pulse and the sustain pulse to apply these pulses to k row electrodes in each sub-block. Fig. 2 only illustrates the driving circuit 5 and the pulse generator 6 for the X-row electrodes, however, it should be noted that a driving circuit and a pulse generator for the Y-row electrodes have the same configuration as the illustrated one.

[0011] The driving circuit 5 includes a driving circuit IC which is indicated by the dotted box 51. For each row electrode, a cathode of a first diode 51A is connected to an anode of a second diode 51B. Anodes of first diodes 51A - 5kA are interconnected. Cathodes of second diodes 51B - 5kB are connected together to the lead 20. A push switch 41 is connected between the anodes of the first diodes 51A - 5kA and the lead 20 which the output from the pulse generator 6 passes through. A plurality of pairs of push switches 31A and 31B, 32A and 32B, ..., 3kA and 3kB are connected in series between a common higher potential and a common lower potential, respectively. A power supply V_H is connected in parallel with the pairs of push switches 31A and 31B, 32A and 32B, ..., 3kA and 3kB. Connecting points between the series push switches 31A and 31B, 32A and 32B, ..., 3kA and 3kB are connected to the cathodes of the first diodes 51A-5kA, the anodes of the second diodes 51B-5kB, and the corresponding row electrodes X_1, X_2, \dots, X_k , respectively. The higher potential terminal of the power supply V_H is connected to the lead 20. A higher potential terminal of the power supply V_H is also connected to a power supply V_S through a switch 52. A lower potential terminal of the power supply V_S is connected to a reference potential.

[0012] When the driving circuit 5 controls the switches 41, 52 simultaneously to open the switch 41 and to close the switch 52, and also controls the switches 31A - 3kA and 31B - 3kB to open and close one of the switches 31A - 3kA and 31B - 3kB alternately, the voltage V_S is applied to the row electrodes X_1, X_2, \dots, X_k , respectively if the push switches 31A - 3kA are closed, otherwise i.e. if the push switches 31B - 3kB are closed, a voltage ($V_S - V_H$) is applied. Therefore, the driving circuit 5 can supply a desired scanning pulse during a

scanning period.

[0013] In the pulse generator 6, a capacitor 70 has one end connected to the reference potential. A switch 45, a coil 61 and a diode 65 are connected in series between the other end of the capacitor 70 and the anodes of the first diodes 51A - 5kA of the driving circuit 5. There is the switch 41 between the diode 65 and the anodes of the first diodes 51A - 5kA. A switch 46, a coil 62 and a diode 66 are connected in series. A cathode of the diode 65 and an anode of the diode 66 are connected to the anodes of the first diodes 51A - 5kA through the switch 41. Further, a power supply V_1 and a push switch 44 are connected in series between the reference potential and the anodes of the first diodes 51A - 5kA through the switch 41. A diode 63 and a push switch 43 are connected in series. The diode 63 is connected with the power supply V_1 in parallel. A higher potential terminal of the power supply V_1 is connected to a cathode of the diode 65 and the anodes of the first diodes 51A - 5kA. The pulse generator 6 generates the priming pulse and the sustain pulse during a priming period and a sustain period, respectively.

[0014] Figs. 3A and 3B illustrate waveforms of the sustain pulses generated by the pulse generator 6. In the following, a process of generating the sustain pulses in the sustain period will be described with reference to Fig. 3A.

[0015] First, assume that all pairs of the push switches 31A - 3kA and 31B - 3kB are opened and the switch 41 is closed. Also, assume that the push switch 44 and the switches 45, 46 are all opened, the push switch 43 is closed, and the output of the pulse generator 6 equals the reference potential.

[0016] Next, when the switch 45 is closed and the switch 43 is opened, a charge current from the capacitor 70 is supplied to the display cells of the PDP through the diode 65 ($t_1 - t_2$). Subsequently, when the switch 45 is opened and the push switch 44 is closed, each of the row electrodes is held at a sustain pulse voltage V_1 ($t_2 - t_3$).

[0017] Next, when the push switch 44 is opened and the switch 46 is closed, discharge currents from the display cells in the PDP are charged on the capacitor 70 through the diode 66 ($t_3 - t_4$). Subsequently, when the switch 46 is opened and the pull switch 43 is closed, the outputs of the respective row electrodes are held to the reference potential.

[0018] By repeating the operations described above, a series of sustain pulses are supplied to the respective row electrodes through the driving circuit 5. As illustrated in Fig. 3B, a sustain pulse for the Y-row electrode is also generated by similar operations. Because its generating timing is shifted by one half of a cycle from the X-sustain pulse, a surface discharge between a pair of the X and Y row electrodes is caused.

[0019] The series of sustain pulses generated by the pulse generator described above are supplied simultaneously to the respective row electrodes, however, each

group of the row electrodes is divided into a plurality of sub-blocks to reduce a required amount of current supplied to each sub-block.

[0020] The number of pairs of row electrodes included in one sub-block is not necessarily the same for every sub-block. For example, sub-blocks positioned near both ends of the panel may be allotted with a larger number of pairs of row electrodes, and sub-blocks in a central area of the panel may be allotted with a smaller number of pairs of row electrodes.

[0021] As described above, since an amount of discharge current required to one driving apparatus IC is reduced, the driving apparatus IC may have a lower power supply capacity, thus facilitating the integration of the driving apparatus into a chip. In addition, since a voltage drop due to the impedance of the lead can be suppressed, the PDP can be utilized as a large screen display.

[0022] Further, the voltage V_1 of the pulse generator 6 determines the output levels of the priming pulse and the sustain pulse. The output terminal of the pulse generator 6, i.e., one end of V_1 is interconnected to those of the respective sub-blocks to maintain the sub-blocks at the same potential level, whereby the levels of the pulses applied to the respective row electrodes are made equal in all the sub-blocks.

[0023] As described above, the group of row electrodes is divided into a plurality of sub-blocks, each of which has one pulse generator to reduce a load on one pulse generator. Also, since the sustain pulses applied to all row electrodes have a constant potential level, the display cells are free from variations in luminance between sub-blocks. A solution is also given to the problem of variations in voltage drop caused due to a variations in impedance of leads which serve as the output terminals of the pulse generators. Furthermore, if any of the pulse generators fails, the pulses are supplied to the sub-block having the failed generator from a pulse generator in any other sub-block. Thus, each of the pulse generators can also serve as a pulse compensating circuit.

[0024] Thus, the present invention has been described with reference to the preferred embodiment thereof. It should be understood by those skilled in the art that a variety of modifications and alterations may be made without departing from the spirit and scope of the present invention. All such modifications and alterations are intended to be encompassed by the appended claims.

Claims

1. A driving apparatus for a plasma display panel comprising:

a group of row electrodes including a plurality of pairs of row electrodes, said group of row electrodes being divided into a plurality of sub-

blocks, each of which includes a plurality of row electrode pairs;

a group of column electrodes including a plurality of column electrodes extending perpendicularly to said group of row electrodes; a pulse generator provided in each of said sub-blocks for generating a sustain pulse; and an electrode driving circuit provided in each of said sub-blocks for selectively relaying said sustain pulse supplied from an output terminal of said pulse generator to apply the relayed sustain pulse to row electrodes in said each sub-blocks, wherein each of said pulse generators has the output terminal connected to those of the rest of said pulse generators.

2. A driving apparatus for a plasma display panel according to claim 1, wherein said pulse generator also generates a priming pulse.

FIG. 1

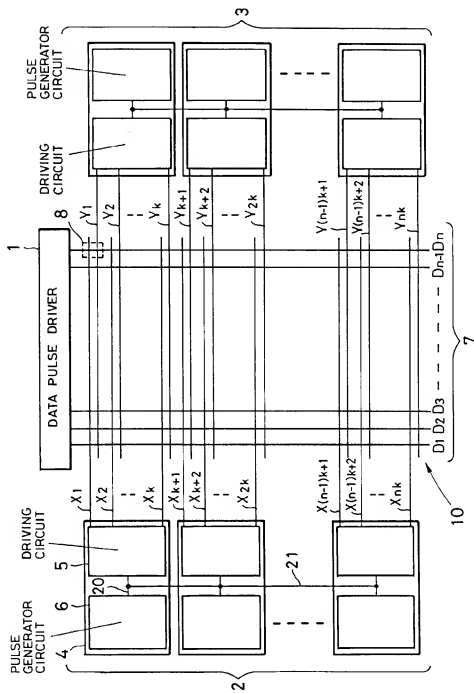


FIG. 2

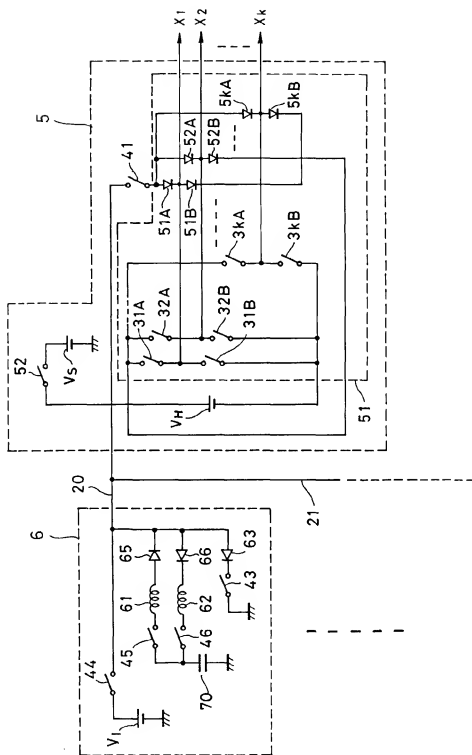


FIG.3A

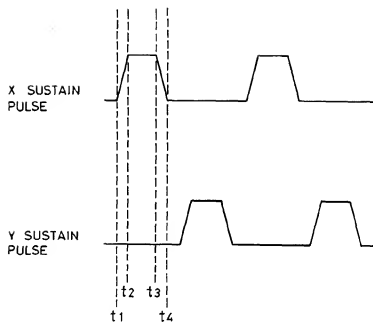


FIG.3B



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 11 1465

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	FR 2 739 480 A (FUJITSU LTD.) 4 April 1997 * abstract * * page 6, line 13 - page 7, line 9 * * page 8, line 14 - line 17; figure 1 * -----	1,2	G09G3/28
A	EP 0 508 053 A (MATSUSHITA ELECTRONICS CO.) 14 October 1992 * abstract * * column 5, line 35 - column 6, line 43; figures 1-3 * -----	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G09G
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 16 November 1998	Examiner O'Reilly, D
CATEGORY OF CITED DOCUMENTS		T theory or principle underlying the invention E earlier patent document, but published on, or after the filing date D document cited in the application L document cited for other reasons & member of the same patent family, corresponding document	
X particularly relevant if taken alone Y particularly relevant if combined with another document of the same category A technological background O non-written disclosure P intermediate document			

EP 0 896 316 A1 (IP/CEN)